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10/804,004	03/19/2004	Makoto Kudo	118768	6984

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EXAMINER	
CONNOLLY, MARK A	

ART UNIT	PAPER NUMBER
2115	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,004	KUDO, MAKOTO	
	Examiner	Art Unit	
	MARK CONNOLLY	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 and 15-16 have been presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-13 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haban[1] in view of Hadji[2] in view of Carter[3].

4. Referring to claim 1, Haban teaches the semiconductor device that accesses at least one semiconductor medium comprising:

a. a bus master [col. 4 lines 35-37].

b. a bus interface that control access to the at least one semiconductor storage medium based on request for access to the at least one semiconductor storage medium from the bus master [108-109 fig. 1 and col. 4 lines 35-39]. Because access to memory is common, the destination is interpreted as comprising a semiconductor storage medium such as SDRAM 108 or SRAM/FLASH/ROM/PCMCIA 109.

c. the at least one semiconductor storage medium including a plurality of semiconductor storage media [fig. 1]. The SDRAM and SRAM are interpreted as the at

[1] As cited in the previous office action.
[2] As cited in the previous office action.
[3] As cited in the previous office action.

least one semiconductor storage medium comprising a plurality of semiconductor storage media.

Although Haban teaches the semiconductor device substantially as claimed above, Haban does not explicitly teach a single bus interface comprising a plurality of dedicated bus interfaces that each correspond to one of the semiconductor storage media and a clock-supply-control circuit that controls the presence of the supply of a clock to the bus interface based on access state information that indicates a state of access to the at least one semiconductor storage medium, the clock-supply-control circuit including a circuit, the circuit implementing at least one control for stopping the supply of the clock to the bus interface if the circuit determines that access is not in execution, and control for supplying the clock to the bus interface if the circuit determines that access is in execution, based on the access state information.

Hadji teaches:

d. the bus interface including a plurality of dedicated bus interfaces that each correspond to a certain one of the semiconductor storage media [abstract, fig. 2, col. 3 lines 35-39 and col. 4 lines 6-12, 34-43]. In particular, bus interface 108 comprises a plurality of buffers 214, 216, 218 and 220 in which each separately interface components with data bus 101. The separate interfaces are interpreted as dedicated bus interfaces corresponding to a certain one of the semiconductor storage media (i.e. buffers 214, 216, 218 and 220).

e. a clock-supply-control circuit that controls the presence of the supply of a clock to the bus interface based on access state information that indicates a state of access to the at least one semiconductor storage medium, the clock-supply-control circuit including a circuit, the circuit implementing at least one control for stopping the supply of the clock

to the bus interface if the circuit determines that access is not in execution, and control for supplying the clock to the bus interface if the circuit determines that access is in execution, based on the access state information [204 fig. 2, col. 2 lines 22-27 and col. 4 lines 33-43].

It would have been obvious to include the interfaces taught by Haban into an interface as taught by Hadji because it would provide a means to reduce the power consumption of the bus interfaces during periods of inactivity in the Haban system as suggested by Hadji [abstract and col. 1 lines 32-36].

Although Haban and Hadji teach independently enabling/disabling the clock to the individual dedicated bus interfaces (i.e. data buffers) within the bus interface based on if the data buffers are active or inactive, it is not explicitly taught that the clock signals are removed from each of the dedicated bus interfaces a predetermined time after each dedicated bus interface completes its access with a first storage medium. In particular, the Haban-Hadji system does not detail how idleness is determined within the system. Carter teaches a well known means to determine idleness in system components by including timers which, when they expire, indicate that components are inactive [col. 2 lines 15-23]. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the timers taught in Carter into the Haban-Hadji system because it would provide a means to determine when the dedicated bus interfaces are idle thus allowing the clocks to the dedicated bus interfaces to be disabled. Although Carter teaches a single timer for controlling the clocks to an entire system when it is determined that the entire system is inactive, it should be apparent that the Haban-Hadji-Carter system would have individual timers for each dedicated bus interface because Hadji explicitly teaches individual

clock control for each dedicated bus interface rather than a system wide control such as that taught in Carter.

5. Referring to claim 2, the Haban-Hadji system teaches:

f. a common bus interface that in common implements operation required for access control when access to any of the plurality of semiconductor storage media is in execution [*Hadji:* interface 108 comprising the clocking units is interpreted as the common bus interface].

g. the plurality of dedicated bus interfaces each correspond to a certain one of the plurality of semiconductor storage media and that each implement operation required for access control only when access to the certain one of the plurality of semiconductor storage media is in execution [*Haban:*108-109 fig. 1 and col. 15 line 62 and col. 16 line 5].

h. the clock-supply-control circuit detects any of the plurality of semiconductor storage media that is other than any of the plurality of semiconductor storage media that is to be accessed based on accessed-medium information indicating which semiconductor storage medium is to be accessed, and controls so as to stop the supply of the clock to any of the plurality of dedicated bus interfaces for the any of the plurality of semiconductor storage media that is other than the any of the plurality of semiconductor storage media that is to be accessed and supply the clock to any of the plurality of dedicated bus interfaces for the any of the plurality of semiconductor storage media that is to be accessed [*Hadji:* abstract].

6. Referring to claim 3, Hadji teaches outputting signals from clock control unit 202 within the bus interface, representative of which clocks to disable [col. 4 lines 33-43]. Each output signal is interpreted as a valid signal.

7. Referring to claims 4-11, these are rejected on the same basis as set forth hereinabove. Hadji teaches a computer system and therefore inherently teaches an input and output device for receiving, processing and outputting information.

8. Referring to claim 12, Carter teaches outputting a signal indicating if activity is detected. If activity is detected, the timer is reset and begins to count the predetermined time again once the activity is over [col. 2 lines 15-23].

9. Referring to claim 13, this is rejected on the same basis as set forth hereinabove.

10. Referring to claim 15, inherently the predetermined time must be longer than one clock cycle because Carter teaches that a time must elapse before determining idleness which indicates that the timer must account for a positive time period. Since everything in a digital system is controlled by clocks, the counting of the timer is also inherently controlled by a clock. In order for the timer to count a given time period, at least one clock cycle must pass to trigger the count operation of the timer.

11. Referring to claim 16, Hadji teaches a cache and system memory being externally located to the bus interface [fig. 1].

12. Claims 1, 3-4, 6-9, 11-13 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hadji in view of Micron[4] in view of Carter.

13. Referring to claim 1, Hadji teaches the invention substantially including:

[4] As cited in the previous office action.

i. a bus interface that controls access to at least one semiconductor storage medium based on request for access to the at least one semiconductor storage medium, the bus interface including a plurality of dedicated bus interfaces that each correspond to a certain one of the semiconductor storage media [abstract, fig. 2, col. 3 lines 35-39 and col. 4 lines 6-12, 34-43]. In particular, bus interface 108 comprises a plurality of buffers 214, 216, 218 and 220 in which each separately interface the system memory 206 or CPU 102 with data bus 101. The separate interfaces are interpreted as dedicated bus interfaces corresponding to a certain one of the semiconductor storage media (i.e. buffers 214, 216, 218 and 220).

j. a clock-supply-control circuit that controls the presence of the supply of a clock to the bus interface based on access state information that indicates a state of access to the at least one semiconductor storage medium, the clock-supply-control circuit including a circuit, the circuit implementing at least one control for stopping the supply of the clock to the bus interface if the circuit determines that access is not in execution, and control for supplying the clock to the bus interface if the circuit determines that access is in execution, based on the access state information [204 fig. 2, col. 2 lines 22-27 and col. 4 lines 33-43].

Although Hadji teaches the invention as claimed above, there is no teaching that the bus interface controls access to the memory based on a request for access by a bus master. Bus masters are well known in the art and are required to control bus access so that multiple devices (like peripherals 110, 112, 114 and 116 or memory devices 214, 216, 218 and 220) do not attempt to communicate over the same bus (data bus 101) at the same time. It is obvious that the Hadji system comprise a bus master for requesting access to the data bus in order to avoid

multiple accesses to the data bus thereby preventing any data corruption which would occur from multiple devices writing to the data bus at the same time.

Lastly, Hadji teaches having at least one system memory (i.e. semiconductor storage medium), but does not explicitly teach that the system memory includes a plurality of semiconductor storage media. Micron teaches that system memory such as SDRAM comprise a plurality of semiconductor storage media [Table 1 and Fig. 1]. For example, Micron teaches that in a 16 Meg memory, the memory will comprise 16 x 1 Meg memory modules, 8 x 2 Meg memory modules or 4 x 4 Meg memory modules. It would have been obvious to one of ordinary skill in the art if not inherent that the system memory in the Hadji system would comprise a plurality of memory modules (interpreted as a plurality of semiconductor storage media) or at least be compatible to use such a memory because system memory such as SDRAM designed by different manufacturers such as Micron use a plurality of memory modules.

As recited above, the Hadji-Micron system teaches a plurality of bus interfaces (buffers 214 and 216) providing an interface between the system memory and data bus 101, and because the system memory comprises a plurality of memory modules, it is interpreted that buffers 214 and 216, because they correspond to the system memory, also correspond to each one of the memory modules in the system memory.

Although Hadji and Micron teach independently enabling/disabling the clock to the individual dedicated bus interfaces within the bus interface based on if the data buffers are active or inactive, it is not explicitly taught that the clock signals are removed from each of the dedicated bus interfaces a predetermined time after each dedicated bus interface completes its access with a first storage medium. In particular, the Hadji-Micron system does not detail how idleness is determined within the system. Carter teaches a well known means to determine

idleness in system components by including timers which, when they expire, indicate that components are inactive [col. 2 lines 15-23]. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the timers taught in Carter into the Hadji-Micron system because it would provide a means to determine when the dedicated bus interfaces are idle thus allowing the clocks to the dedicated bus interfaces to be disabled. Although Carter teaches a single timer for controlling the clocks to an entire system when it is determined that the entire system is inactive, it should be apparent that the Hadji-Micron-Carter system would have individual timers for each dedicated bus interface because Hadji explicitly teaches individual clock control for each dedicated bus interface rather than a global wide control such as that taught in Carter.

14. Referring to claim 3, Hadji teaches outputting signals from clock control unit 202 within the bus interface, representative of which clocks to disable [col. 4 lines 33-43]. Each output signal is interpreted as a valid signal.

15. Referring to claims 4, 6-9 and 11, these are rejected on the same basis as set forth hereinabove. Hadji teaches a computer system and therefore inherently teaches an input and output device for receiving, processing and outputting information.

16. Referring to claim 12, Carter teaches outputting a signal indicating if activity is detected. If activity is detected, the timer is reset and begins to count the predetermined time again once the activity is over [col. 2 lines 15-23].

17. Referring to claim 13, this is rejected on the same basis as set forth hereinabove.

18. Referring to claim 15, inherently the predetermined time must be longer than one clock cycle because Carter teaches that a time must elapse before determining idleness which indicates that the timer must account for a positive time period. Since everything in a digital system is

controlled by clocks, the counting of the timer is also inherently controlled by a clock. In order for the timer to count a given time period, at least one clock cycle must pass to trigger the count operation of the timer.

19. Referring to claim 16, Hadji teaches a cache and system memory being externally located to the bus interface [fig. 1].

Response to Arguments

20. Applicant's arguments filed 1/9/09 have been fully considered but they are not persuasive.

21. In the REMARKS, applicants argue in substance that Hadji does not teach a plurality of dedicated bus interfaces because buffers 214, 216, 218 and 220 (buffers 214 and 216 interpreted by the examiner as a first dedicated interface and buffers 218 and 220 as a second dedicated bus interface) interface with a non-dedicated data bus 101 and also because buffer 216, for example, interfaces with a master peripheral 110 and system memory 106. In addition, applicants also argue that the single timer taught by Carter monitors a plurality of components to determine if a system is active or inactive.

22. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

23. In response to applicant's first argument, although the first dedicated bus interface interfaces with a common data bus 101 does not alleviate the fact that the first dedicated bus interface is dedicated to the system memory (106). In particular, if any of the master or slave peripherals (110, 112, 114 or 116) require access to the system memory, access must be through

the first interface. Because access to the system memory can not go though the second interface but rather requires the first interface, inherently this defines the first interface as being dedicated to the system memory (106). The same argument applies to the second dedicated interface which is dedicated to the CPU (102) for the same reasons. Furthermore, because the first and second dedicated interfaces interface the system memory and CPU respectively to the data bus (101), the interfaces are thus inherently bus interfaces. Therefore, it is reasonable to interpret buffers 214 and 216 as a first dedicated bus interface and buffers 218 and 220 as a second dedicated bus interface.

In addition, one could also interpret the first and second dedicated interfaces as first and second dedicated bus interfaces because the interfaces are not integrated within the system memory and CPU respectively, but rather are part of bus interface (108) and therefore there must exist a first bus dedicated bus coupling the first dedicated interface to the system memory and a second dedicated bus coupling the second dedicated interface to the CPU. In this respect, one can further see that the first and second dedicated interfaces are in fact dedicated bus interfaces.

24. In response to applicant's second argument directed at Carter, it appears that what applicant is doing is ignoring both the Hadji reference and the examiners reasoning in the above rejections. In particular, Hadji teaches determining which interfaces are active and which are inactive in order to individually enable and disable those interfaces. Hadji does not enable and disable the interfaces together, but rather performs the control on an individual basis. What the examiner pointed out though was that even though Hadji broadly suggested that activity and inactivity is determined, the specifics as to how activity and inactivity are determined was not provided by the reference. Carter was then introduced to show that using a timer for counting to zero as long as a plurality of devices are not accessed, can be used to determine inactivity. Even

though Carter is directed to determining system inactivity, it is obvious that the same principles can be applied for determining individual device inactivity since individual device inactivity must be accounted for when determining system wide inactivity.

Conclusion

25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARK CONNOLLY whose telephone number is (571)272-3666. The examiner can normally be reached on M-F 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Mark Connolly/
Primary Examiner, Art Unit 2115
3/6/09

Mark Connolly
Primary Examiner
Art Unit 2115